REMARKS:

Reconsideration and allowance of the pending claims in the application are requested.

Claims 1-32 are pending in the case.

The drawings have been objected to as illegible.

The Abstract has been objected to as exceeding 150 words.

Claims 3-8, 18-22 & 25-32 have been objected to as based on limitations being improperly designated in claims 3 – 8.

Claims 30- 32 have been rejected under 35 USC 112, second paragraph as being substantially duplicates of claims 24-26.

Claims 1-2, 4-5, 13-16, 19, 21, 23, 26, 28-29 and 32 have been rejected under 35 U.S.C. 103(a) as being unpatentable over USP 6,125,415 to E. Liu, issued September 26, 2000, filed June 10, 1998 (Liu), in view of USP 6,332,166 to H. Cranford, Jr. et al., issued December 18, 2001, filed December 15, 1999 (Cranford).

Claims 3, 6, 9-12, 17-18, 20, 22, 24-25, 27 and 30-31 have been rejected under 35 USC 103(a) as being unpatentable over Liu, of record in view of Cranford, of record and in further view of US Publication No. US 2001/0043649 to R. Farjad-Rad, published November 22, 2001, filed May 22, 2001 (Farjad-Rad).

Claim 7 has been rejected under 35 USC 103(a) as being unpatentable over Liu, of record in view of Cranford, of record in further view of USP 4,374,426 to D. Burlage et al., issued February 1983, filed November 14, 1980 (Burlage).

Claim 8 has been rejected under 35 USC 103(a) as being unpatentable over Liu, in view of Cranford, in further view of Burlage and Woodcock Computer Dictionary, 2nd Edition, Microsoft Press, 1994 (Woodcock).

SUMMARY OF CLAIM AMENDMENTS:

Claims 3-8, 18-22, and 25-29 have been amended in the manner instructed by the Examiner.

Claims 30-32 have been canceled as duplicates of Claims 24 -26.

Claims 1, 2, 5, 7, 8, 13, 16, 17, 19, 23 and 24 have been amended to futher define the invention with respect to the cited art.

New Claims 34, 35, and 36 have been added for more detailed protection of the invention.

Before responding to the rejection, applicant would like to distinguish Liu; Cranford; Burlage, and Farjad-Rad from the present invention (Cranford II), as follows:

1. Liu:

Liu discloses a user control system for allowing an end user to control the level of a signal transmitted from a host to a transmission medium, and a method for optimizing the output signal through user control. The user control system includes a digital current controller electrically connected to a bias voltage generator, and formed of a binary weighted transistor array that is switched according to user inputs received from a host. Also disclosed is a transmission system incorporating the user control system and further including a current-mode digital-analog converter, an on-chip low-pass filter, a line driver, and output impedance control. The control system and the method can be used in transmission of Ethernet signals onto an unshielded twisted pair cable. In addition, with appropriate modification, the transmission system and method can be used for transmitting ATM or other signals onto a transmission medium. Liu fails to disclose limitations of Cranford II, as follows:

A. **Liu discloses a driver enabling an end user to control the level of a signal transmitted from a host to a transmission medium and fails to disclose a controllable driver coupled to a transmission medium and overcoming intersymbol interference and other transmission impairments**

Liu discloses a user-controlled driver circuit to control the level of a signal transmitted from a host to a transmission medium. Abstract, lines 1-3. Moreover, Liu fails to combat bandwidth limitations of the channel. In contrast, Cranford II discloses a driver circuit

responsive to coefficient level drivers to overcome intersymbol interference, bandwidth limitations and other transmission impairments. Abstract, lines 1-3.

Liu addresses a different problem, i.e., signal level control and fails to disclose intersymbol interference control and other transmission medium impairments.

B. Liu fails to disclose a transversal filter

Liu discloses a driver circuit responsive to user input to modify the characteristics of a transmission signal. Col. 4, lines 20-30. In contrast, Cranford, II discloses a driver circuit responsive to a transversal filter receiving user inputs to match the inverse of the frequency response of the transmission media. Abstract, lines 16-21.

C. Liu discloses a filter circuit is placed at the input of the line driver and fails to disclose a filter circuit placed at the output of the driver circuit.

Liu, in Fig. 2, discloses a filter 208 at the input of line driver 210. In contrast, Cranford, II discloses a filter circuit connected between a driver circuit and a transmission input.

Liu in view of Cranford describe controlling a current source and fail to overcome transmission impairments.

2. Cranford:

Cranford discloses An adaptive interface and method of operation facilitate connection of a work station in a Local Area Network (LAN) using Shielded Twisted Pair (STP) cabling to an Ethernet 10/100BASE TX installation using Unshielded Twisted Pair (UTP). The work station is coupled through the adaptive interface to the STP cabling system emulating a given number of meters of UTP cabling. The adaptive interface includes programmatically controlled filters interconnecting the RJ 45 and MIC_S connectors. The filter comprises a series of 1 . . . N switchable lumped passive element units which can be sequentially connected into the STP cabling to emulate the amplitude attenuation and phase shift of a preselected length of UTP 5 cabling, typically in the range of 20 meters. In operation, the Physical Layer (PHY) in the communication system enters a start up sequence for the various circuits and cabling in the layer. During the start up sequence, the adaptive interface is bypassed. After an appropriate delay to allow PHY convergence or a bit error rate measurement, the PHY transmit/receive signals are

examined for bit errors by a test unit. If there are no bit errors, no filter element is inserted in the STP cabling by the adaptive interface and the work station is coupled to the Ethernet installation. If there are bit errors, a first filter element is switched into the STP cabling by the adaptive interface. The bit error signals are re-examined. If there are no errors, the workstation is connected to the Ethernet installation. If bit errors continue to exist, the next element(s) of the filter is inserted into the STP cabling until the "Nth" filter element is reached. If bit errors continue to exist on the STP cabling after inserting the Nth filter in the STP cabling, a re-try test sequence is initiated by the adaptive interface and the start up sequence is repeated. If re-try is not initiated, a transmit error is displayed and the workstation/Ethernet installation cannot proceed without modification. A diagnostics menu is displayed and a set-up process determines with human intervention what system changes are needed for the workstation/Ethernet connection. Cranford fails to disclose limitations of Cranford II, as follows:

A. Cranford discloses a switchable lumped passive filter to emulate amplitude, attenuation and phase shift of a pre-selected length of cabling and fails to disclose a transverse or Finite Impulse Response filter controlling transmission line impairments.

Cranford discloses a filter comprising a series of switchable lumped passive elements, which can be sequentially connected into cabling to emulate the amplitude and attenuation, and phase shift of a pre-selected length of cable. Abstract, lines 13-17. In contrast, Cranford, II discloses a transversal filter that functions in the Z-transform mode to control intersymbol interference and other transmission line impairments. Page 10, lines 17-22.

Cranford does not describe a transversal filter. In fact, the term "transversal" does not appear in the Cranford disclosure. Moreover, Cranford is directed to the problem of providing an impedance indicative of a cable length and fails to disclose or suggest the problem of controlling symbol interference on a transmission line.

B. Cranford discloses a single set of switches to control filter elements and fails to disclose multiple sets of control signals for controlling intersymbol interference.

Cranford, at col. 5, lines 11-16, discloses each filter element is controlled by a single switch. In contrast, Cranford, II discloses A and B coefficient setting circuits. The A and

B coefficient circuits control different sides of differential current amplifiers in the driver and power setting circuits for intersymbol interference control. Page 7, lines 16-20.

C. Cranford discloses RC circuits as filter elements and fails to disclose filter elements including shift registers for storing present data input and a history of at least two past data signal inputs.

Cranford, in Fig. 3, discloses each filter element as comprising an RC circuit sequence between input and output. In contrast, Cranford, II discloses each programmable filter element, including a shift register for storing the present signal input and a history of at least two past data signal inputs. Cranford fails to disclose a transversal filter including shift register elements.

3. Burlage:

Burlage discloses a high speed digital equalizer, which provides a means for replacing the conventional transversal filter used to preset equalize a channel with simple digital circuits prior to data transmission. The analog to digital converter and digital multipliers of a transversal filter are replaced with a digital to analog converter and random access memory, respectively, which permit equalizers to be used with band limited channels operating at much higher data rates than previously possible because of sample rate limitations. Burlage fails to disclose limitations of Cranford II, as follows;

A. Burlage discloses a two-stage shift register circuit and fails to disclose a three stage shift register circuit.

Burlage at col. 4, lines 30-47, discloses a data bit is gated into a shift register. Each gate passes a preset coefficient into an Input Summer only if the corresponding register bit is a 1. The sum is held in a buffer of a summer until the beginning of the next timing phase. At the next timing phase, a 0 is clocked into the register and the previous sum is transferred to a D/A converter.

In contrast, Cranford, II at page 12, lines 16 continuing to page 13, line 9, discloses a shift register containing three stages. The shift register contains the outgoing data bit; a history of previous data bits and provides the time delays for FIR filter.

Burlage fails to disclose a three-stage shift register providing time delays in processing data input signals.

B. Burlage discloses holding a single data bit during a clock cycle and fails to disclose holding a history of two or more previous data bits.

Burlage at col. 4, lines 43-47, discloses the sum of the data bits is held in a buffer until the beginning of the next timing post. At the next timing phase, a 0 is clocked into the register and a previous sum is transferred to a D/A converter.

In contrast, Cranford II, at col. 13, line 20 continuing to page 14, line 4 discloses a representative shift register stage includes a balanced latch and a buffer amplifier in each successive stage of the shift register. The balanced latch and buffer amplifier in each phase stage interacts to store the current data pulse and two preceding data pulse. As each data pulse is received, the stored data pulse is shifted out to the next stage and the stage provides a delayed pulse at the ON and OFF terminals of the stage to the transmission line. The buffer stores the data pulse while transferring to one stage to the next.

Burlage fails to disclose three stage shift register storing a history of at least two past data signal bits in the filter.

4. Farjad-Rad:

Farjad-Rad discloses an equalizer including plural samplers for sampling an incoming input data stream according to plural phases of a sampling clock, each sampler producing a data sample. Operating in the analog domain, a multi-tap finite impulse response (FIR) filter weights the data samples and combines the weighted data samples to produce a filtered data bit. The filtered data bits thus form an equalized output data stream. The equalizer can compensate for characteristics of a communications channel, such as low-pass characteristics. The channel may carry high-speed, e.g., multi-gigabit per second, traffic. Farjad-Rad fails to disclose limitations of Cranford 2, as follows:

A. Farjad-Rad describes a multi-tap FIR filter, which combines weighted samples to produce an equalized bit and fails to disclose a FIR filter including shift register

stages controllable by coefficients to match a driver output to the inverse of a transmission line.

Farjad-Rad at paragraphs 47-56, discloses an N-tap FIR filter sampling received data at least once every symbol period at the receiver end . For each received data symbol, its value and previous N-1 symbol values are sampled and held. The N samples are modulated by appropriate filter Tap weights and added or subtracted to produce an equalized data bit. Farjad – Rad criticizes connecting the filter to the transmitter as wasteful of power.

In contrast, Cranford, II, at page 4, line 14 continuing to page 5, line 11 describes an alterable FIR circuit coupled to a driver and including a set of filter coefficients. The driver includes A-coefficient level compensation and B-coefficient level compensation for controlling self induced ISI from the driver, while the filter coefficients are activated. The driver further includes logic to reduce ISI by switching off high capacitance nodes when the filter coefficients are active. Moreover, connecting the filter to the transmitter or driver aids in overcoming cross-talk on the transmission line.

Applicant can find no disclosure in Farjad-Rad relating to connecting a FIR filter to the driver and/or switching a driver off high-capacitance nodes when the filter coefficient is inactive.

B. Farjad-Rad discloses processing successive samples of a data bit to obtain a data bit value and fails to disclose processing a current sample for a data bit value.

Farjad-Rad, at paragraphs 50-52 discloses a plurality of samples of a data stream. Each sample is clocked by a separate phase of a sampling clock. The sample value S_1, a previous sample value S_0 are processed by the output of the previous sample. The output is multiplied by tap weights and the product subtracted from S_1 by an adder. The difference is then sensed by a sensed amplifier as digital bit value.

In contrast, Cranford, II at page 13, line 20 continuing to page 14, line 4, discloses each shift register stage includes a balanced latch and a buffer amplifier. The balanced latch and buffer amplifier interact to store the current data pulse and two preceding data pulses. As each data pulse is received, the stored data pulse is shifted out to the next phase and the stage provides the delayed pulse to the transmission line.

Farjad-Rad fails to disclose processing a current sample for a data bit value.

5. Summary:

Summarizing, Liu, in view of Cranford, and in further of view of Farjad-Rad and Burlage do not teach, disclose or suggest a driver circuit coupled to (a) a transversal FIR, including (i) multiple coefficient setting circuits processing data bits via (ii) three stage shift registers to obtain time delays obtain based on a Z transform to alter the frequency response of the driver to match the inverse of the frequency response of a transmission medium, and (b) coefficient compensation circuits for correcting driver self-induced ISI while the filter coefficients are activated. Without such teaching, there is no basis for a worker skilled in the art to implement claims 1-29. The rejection of claims 1-29 under 35 USC 103(a) based on the cited art is without support. Withdrawal of the rejection and allowance of claims 1-29 are requested.

RESPONSE TO INDICATED PARAGRAPHS OF THE REJECTION:

Response to Paragraph 1:

Applicant notes the status of the claims

Response to Paragraph 2:

Applicant submits herewith Replacement Sheets for Figs. 1-1, which are in compliance with 37 CFR 1.84. The Replacement sheets are believed to satisfy the requirement for corrected drawings.

Response to Paragraph 3:

Applicant submits herewith a Substitute Abstract which complies with 37 CFR 1.72 and overcomes the Examiner's objection. Withdrawal of the objection to the Abstract is requested.

Response to Paragraph 4:

Dependent claims 3-8, 18-22 and 25-32 have been amended as directed by the Examiner. Withdrawal of the objection is requested.

Response to Paragraph 5/6:

Claims 30 – 32 have been canceled.

Response to Paragraph 7/8:

Claims 1-2, 4-5, 13-16, 19, 21, 23, 26, 28-29 include limitations not disclose or suggested in Liu in view of Cranford, as follows:

a. Claim 1:

(i) "a controllable driver set coupled to a transmission media and including compensation means compensating for a self induced ISI;"

Applicant can find no disclosure in Liu for Cranford describing a driver, including compensating for self induced ISI, as described in the specification at page 15, lines 1-16.

(ii) "a transversal filter receiving a data input signal and coupled to the transmission media, the filter having programmable filter coefficient sets;"

Liu does not disclose a transversal filter. Cranford, at col. 4, line 10-30, describes a single set of filter elements programmably switchable into an STP cable to change the attenuation and of phase of the signal on the STP cabling for transmitting Ethernet signals on UTP cabling. In contrast, Cranford, II, at page 11, line 3 continuing to page 12, line 15, describes a transversal filter including A-coefficient and a B-coefficient setting circuits for controlling intersymbol interference on different sides of a transmission line..

Liu and Cranford fail to disclose multiple coefficient setting circuits for controlling both sides of a transmission line.

(iii) "means for altering a frequency response of the controller driver set based on a Z transform to match the inverse of the frequency response the transmission media."

Cranford, at col. 5, lines 3-46, discloses filter circuits programmably connected in series to provide an equivalent length of UTP cabling such that there is sufficient attenuation to appear as Ethernet signals on the UTP cabling.

In contrast, Cranford, II, at page 10, describes a Z transform function controlled by A and B coefficient setting circuits to modify the frequency response of the driver.

Liu and Cranford fail to disclose modifying the driver to match the inverse of the frequency's response of the transmission media via multiple coefficient setting circuits.

Summarizing, Liu and Cranford, alone or in combination, do not disclose or suggest a driver, including (a) compensation means for correcting self-induced ISI; (b) a transversal filter having programmable coefficient sets, and (c) altering the frequency response of the driver based on a Z transform to match the inverse of the frequency response of the transmission media. The prior art does not teach, disclose or suggest the elements of claim 1 and without such teaching or disclosure, the rejection of claim 1 under 35 USC 103(a) fails for a lack of support in the prior art. Withdrawal of the rejection and allowance of claim 1 are requested.

b. Claim 2:

(i) "means including the compensation means providing constant output peak amplitude on the transmission media independent of the programmable filter coefficient."

Applicant can find no disclosure in Liu relating to implementing the control system to transmit constant power over the transmission media independent of the switchable filter elements of Cranford. In contrast, Cranford, II, at page 17, line 17 continuing to page 18, line 3, describe the compensation circuit subtracting out the exact amount of current from the main current source as the active coefficients are using enabling the maximum currents to be held to a constant amplitude for a given power level setting.

The prior art fails to disclose providing a constant output peak amplitude independent of the programmable filter coefficient.

(c) Claim 4:

Claim 4 further limits claim 1 and is patentable on the same basis thereof.

(d) Claim 5:

(i) "means responsive to the programmable filter coefficient sets, each set providing control signals to the transmission line for matching the controller driver set output to the inverse of the transmission media."

Cranford discloses in Fig. 2, a single set of filter elements programmably switchable into an STP cable to change the attenuation and phase of the signals on the STP cabling transmit to represent Ethernet signals on UTP cabling. In contrast, Cranford, II, at page

9, line 22 continuing to page 10, line 21, discloses a set of coefficient setting circuits modifying the frequency response of the driverbased on a Z transfer function. Cranford fails to disclose a set of programmable filter coefficients, each providing control signals to the transmission line for matching the control of the driver output to the inverse of the transmission medium.

The prior art does not disclose or suggest programmable coefficient sets, each connected to the transmission lines. Without such support, there is basis for a worker skilled in the art to implement claim 5. The rejection of claim 5 under 35 USC 103(a) fails for lack of support in the prior art. Withdrawal of the rejection and allowance of claim 5 are requested.

(e) Claim 13:

Claim 13 is patentable on the same basis as claim 5.

(f) Claim 14:

Claim 14 is patentable on the same basis as claim 1.

(g) Claim 15:

Claim 15 is patentable on the same basis as claim 2.

(h) Claim 16:

(i) "connecting a controllable driver set to an input node and to a transversal filter including a set of programmable coefficients coupled to a transmission medium;"

Liu, Cranford, Farjad-Rad and Burlage all fail to disclose a set of programmable coefficients coupled to a transmission medium.

(ii) "compensating the driver for self induced driver ISI"

Applicant can find disclosure in Liu, Cranford, Farjad-Rad and Burlage where the driver self-induced ISA is compensated by compensation circuit, as described in Cranford II in at page 15, lines 1-16.

(i) Claim 19:

Applicants can find no disclosure in Liu, in view of Cranford reducing self induced intersymbol interference by turning off the output transistors to reduce the output capacity mode, as described in the specification at page 16, lines 16-17.

(j) Claim 21:

Claim 21 is patentable on the same basis as claim 16.

(k) Claims 23-29:

Claim 23-29 are the program product implementations of claims 16-22. Claims 23-29 are patentable on the same basis as claim 16-22.

Summarizing, claims 1-2, 4-5, 13-16, 19, 21, 23, 26, 28-29 describe limitations not disclosed in Liu in view of Cranford, as discussed above. Without a teaching describing the limitations, there is no basis for a worker skilled in the art to implement the rejected claims. Withdrawal of the rejected claims under 35 USC 103 (a) and allowance thereof are requested

Response to Paragraph 9:

Claims 3-6, 9-12, 17-18, 20, 22, 24-25, and 27 include limitations not disclosed or suggested in Liu in view of Cranford and in further view of Farjad-Rad, as follows:

(a) Claim 3:

(i) "logic means for switching the transversal filter and controllable drivers off high capacitance node when the programmable filter coefficients are inactive."

Farjad-Rad, at paragraphs 50-56, describes a FIR filter processing data samples to cancel intersymbol interference caused in the channel. Cranford, II can find no disclosure in Farjad-Rad relating to switching the transversal filter and controllable drivers off the high capacitance nodes when the programmable filter coefficients are inactive, as described in the specification at page 12, lines 1-7.

Liu and Cranford fail to disclose or teach a worker skilled in the art to implement claim 3. The rejection of claim 3 fails for lack of support in the prior art. Withdrawal of the rejection and allowance of claim 3 are requested.

(b) Claim 6:

(i) "means for storing a present data input signal bit and a history of at least two past data signal input bits in a transversal filter."

Farjad-Rad, at col. 50-56 discloses a FIR equalizer processing a current signal and a past signal to determine the value of a data bit. In contrast, Cranford, II, discloses at page 12, lines 16-20, shift register processing a current bit and storing a history of previous data bits. Farjad-Rad fails to disclose storing the current data bit and two previous data bits.

(c) Claim 9:

Liu, Cranford and Farjad-Rad all fail to disclose a Z function mode in processing data bits to reduce intersymbol interference.

(d) Claim 10:

Claim 10 is patentable on the same basis as claim 1.

(e) Claim 11:

Claim 11 is patentable on the same basis as claim 1.

(f) Claim 12:

Claim 12 is patentable on the same basis as claim 1.

(g) Claim 17:

Claim 17, as amended, is patentable on the same basis as claim 6.

(h) Claim 18:

Claim 18 is patentable on the same basis as claim 16.

(i) Claim 20:

Claim 20 is patentable on the same basis as claim 3.

(j) Claim 22:

Claim 22 is patentable on the same basis as claim 16.

(k) Claims 24 – 25:

Claims 24 and 25 are the program implementation of claims 17 and 18 and are patentable on the same basis thereof.

(l) Claim 27:

Claim 27 is the program implementation of claim 20 and is patentable on the same basis thereof.

Summarizing, claims 3, 6, 9-12, 17-18, 20, 22, 25-25 and 27 include limitations not disclosed in Liu in view of Cranford and in further view of Farjad-Rad, as discussed above. Without a teaching in the prior art, there is no basis for a worker skilled in the art to implement the rejected claims . Moreover, the Examiner has not disclosed any predictability of success in combining the references, as required by MPEP 2143.02. Withdrawal of the rejection under 35 USC 103 (a)0 and allowance of the rejected claims are requested.

Response to Paragraph 10:

Claim 7 includes limitations not disclosed or suggested in Liu in view of Cranford and in further view of Burlage, as follows:

(a) Claim 7:

(i) "three stage shift register elements in a transversal filter providing time delays and processing the data input signal."

Cranford, in Fig. 5, Farjad-Rad, in Fig. 5, and Burlage in Fig. 2, all fail to disclose a three-stage shift register element shown in Fig. 7, and described at page 12, line 16 continuing to page 13, line 9.

Response to Paragraph 11

Claim 8 includes limitations not disclosed or suggested in Liu, in view of Cranford in further view of Burlage and Woodcock, as follows::

(a) Claim 8:

(i) "buffer and latch means in each stage of a three stage shift register in a transversal filter for storing data impulse signals in time sequence."

Claim 8 is patentable for the same reasons as described in connection with the consideration of claim 7.

PATENTABILITY SUPPORT FOR NEW CLAIMS 33-35:

Claim 33 describes the transmission line in claims 1 and 16 as providing true and complement outputs. The A coefficient circuit control one side of the transmission line and the B coefficient circuit control the other side of the transmission line for intersymbol interference reduction.

Claims 34 – 36 further limit claim 33 by (i) a power down circuit, which switches the filter components off high capacitance nodes when the filter coefficients are inactive, and (ii) a power down signal lowering the power applied to transmission lines by an output amplifier and switching off and out put current source transistor to provide a high impedance to ground.

Applicant can find no disclosure in Liu, Cranford, Farjad-Rad and Burlage incorporating a transmission line with true and complement lines matched to a controllable driver and a power down circuit as described in claims 33 - 36 for reducing intersymbol interference.

Entry and allowance of claims 33-36 are requested.

CONCLUSION:

Having provided corrected drawings; limited the Abstract to 150 words; overcome the objections and rejections under 35 USC 112/2; distinguished claims 1-29 from the cited art and supported the patentability of new claims 33-36, Applicants request entry of the amendment, allowance of claims and passage to issue of the case.

AUTHORIZATION:

The Commissioner is hereby authorized to charge any fees or insufficient fees or credit any payment or overpayment associated with this application to IBM Deposit Account No. 50-0563, Order No. RAL920000097US1 (1963-7408).

Respectfully submitted,

MORGAN & FINNEGAN, O.K.

Dated: September 28, 2004

By: Joseph C Redmond Jr

Joseph C. Redmond, Jr.
Reg. No. 18,753
Telephone: (202) 857-7887
Facsimile: (202) 857-7929

CORRESPONDENCE ADDRESS:

Morgan & Finnegan LLP.
3 World Financial Center
New York, NY 10281-2101